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Brief 9/21/01

PATENT
Attorney Docket No. 401251/TAKADA

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

ISHIDA et al.

Art Unit: Unassigned

Application No.: Unassigned

Examiner: Unassigned

Filed: June 11, 2001

For: MATCHING CIRCUIT AND SEMICONDUCTOR DEVICE

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Prior to the examination of the above-identified patent application, please enter the following amendments and consider the following remarks.

IN THE SPECIFICATION:

Replace the paragraph beginning at page 1, line 14 with:

In mobile radio communications between such mobile terminals as portable phones, both communication speed and communication capacity have been increased along with an increase of the information content. That is, the use of higher frequencies is required as those communication frequencies. In the case where a high frequency is used as a communication frequency, the importance of a matching circuit for matching between input and output parts or between transistors is becoming higher. This is because a high frequency circuit is degraded in both output and efficiency, as well as its noise increases and the frequency band is changed when the capacitance of a capacitor, the inductance of an inductor, or the electrical property of the transistor included in this

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SPECIFICATION, CLAIMS AND ABSTRACT AS PRELIMINARILY AMENDED

Amendments to the paragraph beginning at page 1, line 14:

In mobile radio communications between such mobile terminals as portable phones, both communication speed and communication capacity have been increased along with an increase of the information content. That is, the use of higher frequencies is required as those communication frequencies. In the case where a high frequency is used as a communication frequency, the importance of a matching circuit for matching between input and output parts or between transistors is becoming higher. This is because a high frequency circuit is degraded in both output and efficiency, as well as its noise increases and the frequency band is changed when the ~~capacity value~~ capacitance of ~~the~~a capacitor, the inductance ~~value~~ of ~~the~~ an inductor, or the electrical property of the transistor included in this matching circuit is shifted from the design value. Especially, this phenomenon appears remarkably in frequency bands referred to as millimeter wave bands over 30GHz.

Amendments to the paragraph beginning at page 1, line 27:

In the case where a high frequency band is used, a matching circuit must be ~~formed around~~ located close to a ~~pole~~ lead of each transistor, since ~~frequency~~

wavelengths are short in ~~such~~ high frequency bands such as millimeter wave bands. In spite of this, it is actually impossible to form such a matching circuit outside a semiconductor substrate. Generally, therefore, a monolithic microwave integrated circuit (MMIC) is employed for mobile radio communications, since it is formed together with a matching circuit on the same substrate. The MMIC mentioned here means a plurality of microwave circuits formed on one semiconductor chip after the respective microwave circuits are assembled with parts.

Amendments to the paragraph beginning at page 2, line 5:

Figs. 10(A) and 10(B) show two examples of a conventional input side matching circuit. In Fig. 10(A), reference numeral 5 denotes an input terminal, reference numerals 10 and 12 denote lines, reference numeral 26 denotes a transistor, reference character L1 denotes an open stub ~~capacity~~ capacitance (of the line 10), and reference character L2 denotes an inductance of the line 12. In Fig. 10(B), reference numeral 5 denotes an input terminal, reference numeral 12 denotes a line, reference numeral 26 denotes a transistor, reference numeral 38 denotes a capacitor, reference character C1 denotes an MIM ~~capacity~~ capacitance (a total ~~capacity~~ capacitance of the three layers; metal, insulator, and metal layers) of the capacitor 38, and reference character L2 denotes an inductance of the line 12. Reference character a denotes a point for denoting a gate-source ~~capacity~~ capacitance when the point is viewed from the input side of the transistor 26, reference character c denotes a point when it is viewed together with the inductance L2, and reference character d denotes a point when it is viewed together with the open stub ~~capacity~~ capacitance L1 from the input terminal 5. As shown in Figs. 10(A) and 10(B), the capacitor C1, etc. having an MIM ~~capacity respectively~~ capacitance and the transistor 26 are patterned on the same substrate.

Amendments to the paragraph beginning at page 2, line 22:

Fig. 11 is a Smith chart for an input side matching circuit shown in Fig. 10. In Fig. 11, the same reference numerals are given to the same items as those shown in Fig. 10, avoiding redundant description. In Fig. 11, reference symbol Cgs denotes a simplified gate-source ~~capacity~~ capacitance seen typically in an input side equivalent

circuit of the transistor 26. As shown in Fig. 11, the impedance, at the time of viewing it from the input terminal 5 side in the design stage, moves to the point d on the Smith chart. The point d denotes 50Ω obtained by combining the gate-source ~~capacity~~ capacitance Cgs, the inductance L2, and the open stub ~~capacity~~ capacitance L1 or MIM ~~capacity~~ capacitance C1.

Amendments to the paragraph beginning at page 2, line 31:

As described above, the MMIC enables both of the capacitor C1 having an MIM ~~capacity~~ capacitance and the transistor 26 to be formed on the same substrate, so an excessive insulation film (MIM insulation film) is formed unavoidably around the transistor 26 due to the fabrication method. Consequently, this excessive insulation film generates a parasitic ~~capacity~~ capacitance, causing the electrical property of the transistor 26 to be changed. Table 1 shows results of a comparison performed with respect to ~~such~~ the parasitic ~~capacity~~ capacitance at input side and output side of the transistor 26 between when an MIM insulation film is formed and when not formed around the transistor 26.

Amendments to the paragraph beginning at page 3, line 11:

As shown in Table 1, the ~~capacity~~ capacitance Cgs[pF/mm] at the input side of the transistor 26 is 0.73[pF/mm] when no MIM insulation film is formed around the transistor 26 while it becomes 0.89[pF/mm] when an MIM insulation film is formed around the transistor 26. The ~~capacity~~ capacitance Cgs[pF/mm] at the output side of the transistor 26 is 0.16[pF/mm] when no insulation film is formed around the transistor 26 while it becomes 0.22[pF/mm] when an MIM insulation film is formed around the transistor 26. That is, in the case where the MIM insulation film taken as an MIM ~~capacity~~ capacitance changes due to the unevenness among fabrication processes, the ~~capacity~~ capacitance components at both input and output sides of the transistor 26 are changed, thereby the matching point is shifted from the design ~~one~~ and the property of the subject high frequency circuit changes. Hereinafter, this high frequency circuit property change will be described with respect to the input side impedance with reference to the Smith chart shown in Fig. 11. In Fig. 11, when the MIM insulation film is thick, the input side

~~capacity~~ capacitance Cgs of the transistor 26 increases, so that the point a on the design is shifted to the point a' and the point c is shifted to the point c' due to the inductance L2. The input side impedance obtained when the inductance L2 is combined with the open stub ~~capacity~~ capacitance L1 or MIM ~~capacity~~ capacitance C1 is also shifted to the point d'. The impedance is thus shifted from the matching point.

Amendments to the paragraph beginning at page 4, line 6:

On the other hand, when the matching circuit uses the MIM ~~capacity~~ capacitance C1, a relationship denoted by the following Equation 1 is assumed between the MIM insulation film thickness L and the MIM ~~capacity~~ capacitance C1.

Amendments to the paragraph beginning at page 4, line 11:

Here, C1 denotes an MIM ~~capacity~~ capacitance, ε denotes an inductance rate of the MIM insulation film, S denotes a pattern area of the MIM capacitor C1, and L denotes an MIM insulation film thickness. As shown in the expression 1, when the MIM insulation film thickness L increases, the MIM ~~capacity~~ capacitance C1 decreases. On the Smith chart shown in Fig. 11, therefore, the input side impedance is further shifted to the point d", thereby the impedance is further shifted from the matching point.

Amendments to the paragraph beginning at page 4, line 18:

According to the above description, it is considered that the same phenomenon also occurs for the output side impedance when the input side ~~capacity~~ capacitance Cgs is replaced with the output side ~~capacity~~ capacitance Cgd. That is, the impedance is shifted from the matching point due to a change of the MIM insulation film thickness L.

Amendments to existing claims:

1. (Amended) A matching circuit for absorbing fluctuation of ~~electric~~ electrical characteristics of a transistor, comprising ~~:~~ a capacitor having a ~~capacity~~ capacitance that increases and decreases ~~contrarily~~ opposite to ~~increment and decrement of~~ changes in a parasitic ~~capacity around~~ capacitance at said transistor.

2. (Amended) The matching circuit according to claim 1, wherein ~~said~~ the parasitic ~~capacity~~ capacitance increases and decreases according to a thickness change of an MIM insulation film ~~formed~~ located around said transistor and said capacitor has an MIM ~~capacity to increase~~ capacitance that increases and ~~decrease contrarily~~ decreases opposite to ~~the increment and decrement of said~~ changes in the parasitic capacity.

3. (Amended) The matching circuit according to claim 2, wherein said capacitor is ~~provided~~ located at an input side of said transistor.

4. (Amended) The matching circuit according to claim 3, ~~wherein said matching circuit is provided with~~ comprising a ~~predetermined~~ bias circuit ~~disposed~~ connected in parallel ~~to~~ with said capacitor ~~provided at the input side of said transistor~~.

5. (Amended) The matching circuit according to claim 2, wherein said capacitor is ~~provided~~ located at an output side of said transistor.

6. (Amended) The matching circuit according to claim 5, ~~wherein said matching circuit is provided with~~ comprising a ~~predetermined~~ bias circuit ~~disposed~~ connected in parallel ~~to~~ with said capacitor ~~provided at the input side of said transistor~~.

7. (Amended) The matching circuit according to claim 2, wherein said capacitor is ~~provided~~ located at an input side of said transistor.

8. (Amended) The matching circuit according to claim 7, ~~wherein said matching circuit is provided with~~ comprising a ~~predetermined~~ bias circuit ~~disposed~~ connected in parallel ~~to~~ with said capacitor ~~provided at the input side of said transistor~~.

9. (Amended) The matching circuit according to claim 2, wherein said capacitor is ~~provided~~ located at an output side of said transistor.

10. (Amended) The matching circuit according to claim 7, ~~wherein said matching circuit is provided with~~ comprising a ~~predetermined~~ bias circuit ~~disposed~~ connected in parallel ~~to~~ with said capacitor ~~provided at the input side of said transistor~~.

11. (Amended) A semiconductor device ~~fabricated with use of~~ including said matching circuit according to claim 1.

12. (Amended) A semiconductor device ~~fabricated with use of~~ including said matching circuit according to claim 2.

Amendments to the abstract:

Abstract of the Disclosure

A matching circuit that can protect a high frequency circuit from degradation in both output and efficiency, as well as from an increase of noise, and changes of a frequency band even when an MIM insulation film thickness ~~L~~ around a subject transistor changes due to an unevenness among fabrication processes~~, thereby~~. As a result, an electrical property of the transistor never changes among products~~, and provide a semiconductor device that employs such the matching circuit~~. An MIM ~~capacity C1~~ capacitance is connected to an input side of the transistor so as to be combined with an input ~~capacity~~ capacitance of the transistor~~, thereby changes~~. Changes of the MIM insulation film thickness ~~L~~ can be eliminated automatically. The MIM ~~capacity C1~~ capacitance changes ~~contrarily~~ opposite to the changes of the MIM insulation film thickness ~~L~~. That is, it is possible to realize a matching circuit that can absorb ~~fluctuation~~ fluctuations of electric characteristics of the subject transistor automatically ~~while~~ when the fluctuation of electric characteristics of the transistor are caused by changes of the MIM insulation film thickness ~~L~~ around the transistor ~~to occur~~ due to ~~the unevenness among~~ non-uniformities in fabrication processes. In addition, ~~in the case~~ where the matching circuit ~~is provided with~~ includes a bias circuit, it is possible to obtain a high frequency circuit that can operate stably in a wide frequency band.

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CLAIMS PENDING AFTER PRELIMINARY AMENDMENT

1. A matching circuit for absorbing fluctuation of electrical characteristics of a transistor, comprising a capacitor having a capacitance that increases and decreases opposite to changes in a parasitic capacitance at said transistor.

2. The matching circuit according to claim 1, wherein the parasitic capacitance increases and decreases according to a thickness change of an MIM insulation film located around said transistor and said capacitor has an MIM capacitance that increases and decreases opposite to changes in the parasitic capacity.

3. The matching circuit according to claim 2, wherein said capacitor is located at an input side of said transistor.

4. The matching circuit according to claim 3, comprising a bias circuit connected in parallel with said capacitor.

5. The matching circuit according to claim 2, wherein said capacitor is located at an output side of said transistor.

6. The matching circuit according to claim 5, comprising a bias circuit connected in parallel with said capacitor.

7. The matching circuit according to claim 2, wherein said capacitor is located at an input side of said transistor.

8. The matching circuit according to claim 7, comprising a bias circuit connected in parallel with said capacitor.

9. The matching circuit according to claim 2, wherein said capacitor is located at an output side of said transistor.

10. The matching circuit according to claim 7, comprising a bias circuit connected in parallel with said capacitor.

11. A semiconductor device including said matching circuit according to claim 1.

12. A semiconductor device including said matching circuit according to claim 2.